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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,293	08/27/2003	Hedley James Francis	550-450	4462

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,293	FRANCIS ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-62 are presented for examination.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 43-62 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The computer program product is directed to a program per se. The evidence shows that applicant's embodiment can be done in mixed hardware and software, and it can be also done in pure software (see page 15, lines 6-13). Furthermore, no specific elements of the program product have been reflected into the claim body to support the program product in the preamble. Therefore, program product is read as a mere program. Hence, no useful , concrete , and tangible results can be determined.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-17,21-38, 42-58,62 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohshima (5,598,544).

4. As to claim 1, 22,43, 43, Ohshima disclosed at least :

a) detecting an attempt to execute a variable length instruction spanning two discrete memory address regions (see fig.7A) , the two discrete memory address regions (see the basic segment 1 and basic segment 2) being a current memory address region and a following memory address region (see also fig. 515 to see how pointer P was used to address leading end of segment in the memory 403);

b) concatenating instruction data from an end portion of the current memory address region and a start portion of following memory address region into a fix-up memory address region of said memory (see the read out position by pointer P in col.2, lines 38-50) to form concatenated instruction data containing said variable length instruction (instruction code unit length, see also the concatenation of instruction fields in fig.1 and fig.5 , see also fig.7B);

(diverting program execution flow to execute the current variable length instruction from within the concatenated instruction data in the fix-up memory address region (see the execution unit 13 in fig.4 and fig.8C, for fixed up address see rearranged P pointer); and

(iv) restoring program execution flow to execute instructions (execution not explicitly shown, but see execution unit [13] in 4) following the variable length instruction from

within following memory address region (see next instruction segment in the memory region [404] in fig.5).

5. The two basic segments were at discrete addresses because the corresponding expanded segment had a variable length (see 7, lines 1-5). Therefore, the second basic segment could start at any position. Also the first basic segment was shown to have a random position in fig.7A. See also variable instruction length in the background in col.1, lines 14-27.

6. As to claim 22, claim 2 is directed to the same scope as claim 1 in apparatus .

7. As to claim 43, claim is directed the same scope as claim 1 in program product format. The examiner holds that this program product is not given a patentable weight because no specific recitation in the body of the claim reflects the specific elements of the program product.

8. As to claim 2,23, Ohshima also included hardware control (see fig.11).

9. As to claim 3, 24, Ohshima also included software control (see micro ROM control in col.7, lines 40-42, see also PLA).

10. As to claims 4,25,45, 46, the structural relation between the memory and the instruction buffer has been reflected into the claim, therefore, Ohshima also included instruction buffer (see the instruction buffer in fig.6A, this instruction buffer include the instruction storage 403, see also readout buffer at the output of storage 3 in fig.7B)

11. As to claims 5,26,47, see instruction fetched from the memory [430] to an instruction buffer [instruction register] before being executed in fig.4).

As to claims 6,27, Ohshima also included sequential addresses (see the entry 404 404' 404").

12. As to claims 7,8,27,28,29, 48,49, Ohshima also marked the valid instruction (see the marking for indicate whether to simultaneously decode the segments in col.7, lines 54-65, col.10, lines 28-48).

13. As to claims 9, 30, 50, Ohshima also disclosed a program counter (see program counter in col.2, lines 41-43).

14. As to claims 10,31,51, see how the program counter P readjusted to the leading position in col.8, lines 10-53).

15. As to claims 11,12, 13, 14,32,33,34, 35,52,53,54, 55, for the flag for single variable instruction length , see the instruction unit length in col.2, lines 48-50, see the L in the position identifying circuit in col.15, lines 56-58, col.16, lines 1-9).

16. As to claims 16,17, 36,37,38, 56, 57, 58, Ohshima also to point to the next instruction following the current instruction (see how the use of pointer 7 to point each

of the 7 fields in a given entry 4 in col.8, lines 10-23, for calculation , see calculation of address in col., lines 40-54 for background) . AS to the diversion, it is read as pointer action (see the pointer P of Ohshima).

17. As to claims 21, 42, 62, see instruction storage 403 in fig.4.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 18-20, 39-41, 59-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohshima (5,598,544) in view of Komatsu (6,324,686) .

19. As to claims 18-20,39-41,59-61, limitations of parent claims 1,22 have been discussed above, therefore, will not be repeated herein. Ohshima did not teach the java byte code as claimed. However, Komatsu disclosed a java byte code of variable length (see col.1, lines 56-60). It would have been obvious to use the java bycode as claimed because the use of Komatsu could provide Ohshima the ability to process his variable length instruction in a different type of language , such as the bycodes, or like, and therefore, increasing the control adaptability of Ohshima, and because Ohshima already taught the rearrangement of his variable length instruction fields , one of ordinary skill in the art should be able to recognize the applicability of partitionable program codes, such as the byte codes , which was already taught by Komatsu to be

used in a variable length instruction, into Ohshima in order to enhance the system compatibilities, and for doing so, provide a motivation.

20. As to the further instruction set in claim 19 , Komatsu also included a further instruction set (see C++ programming in col.1, lines 30-35.

21. As to the branch in claim 20, Ohshima already taught branch (see jump in col.7, lines 54-65).

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Philips et al. (6,237,074) is cited for the teaching of concatenating variable instruction length with the starting position pointers (see col.14, lines 36-61);

b) Wang et al. (US2004/0268326) is cited for the teaching of java bytecode instruction spanning in discrete regions (see the code blocks 22 to 28, in separate cache lines in fig.5, Paragraph 0032);

c) Zou et al. (6,425,070) is cited by applicant, and it shows the concatenation of instruction fragments (see col.8, lines 1-45).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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